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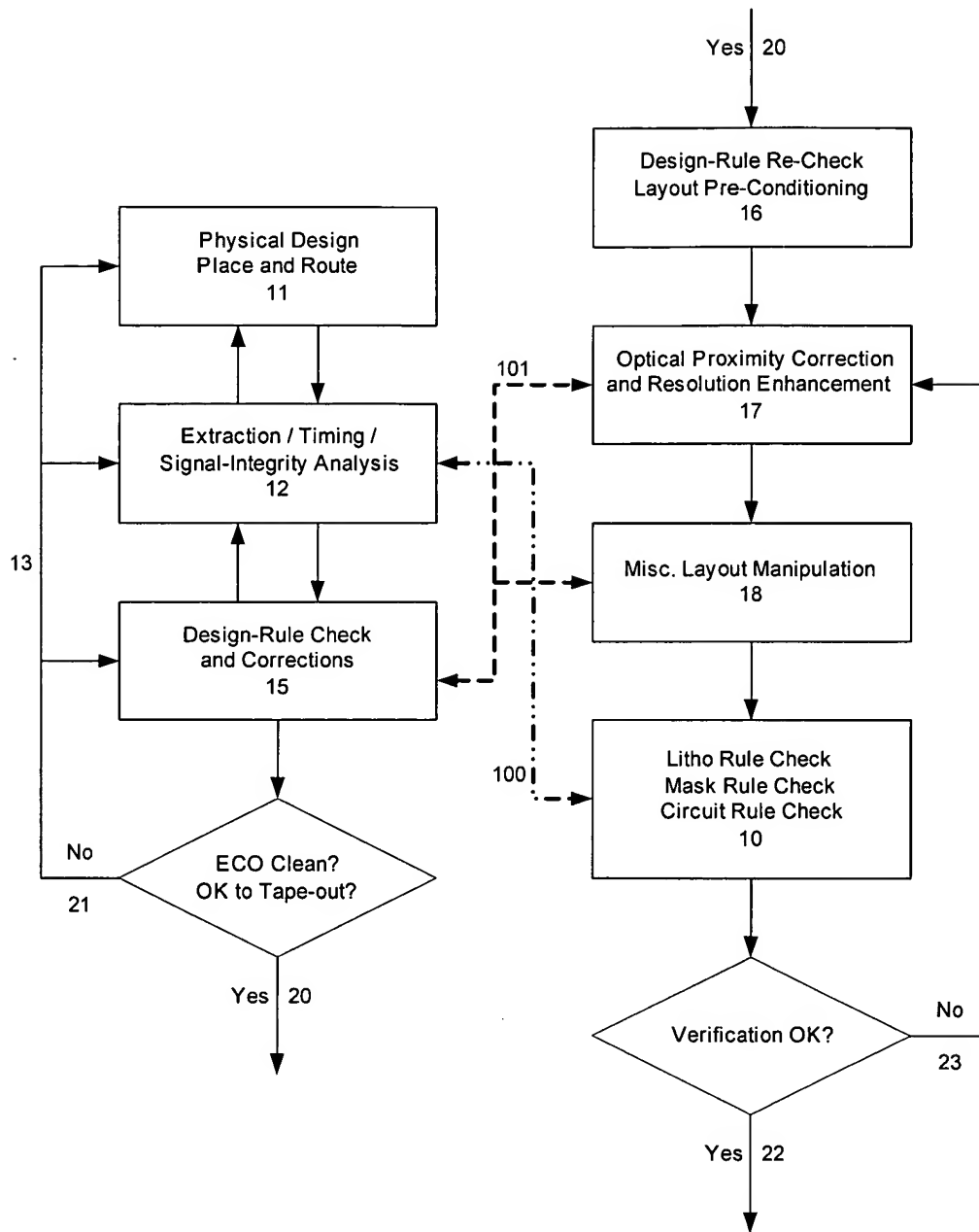


Figure 1a

Figure 1b

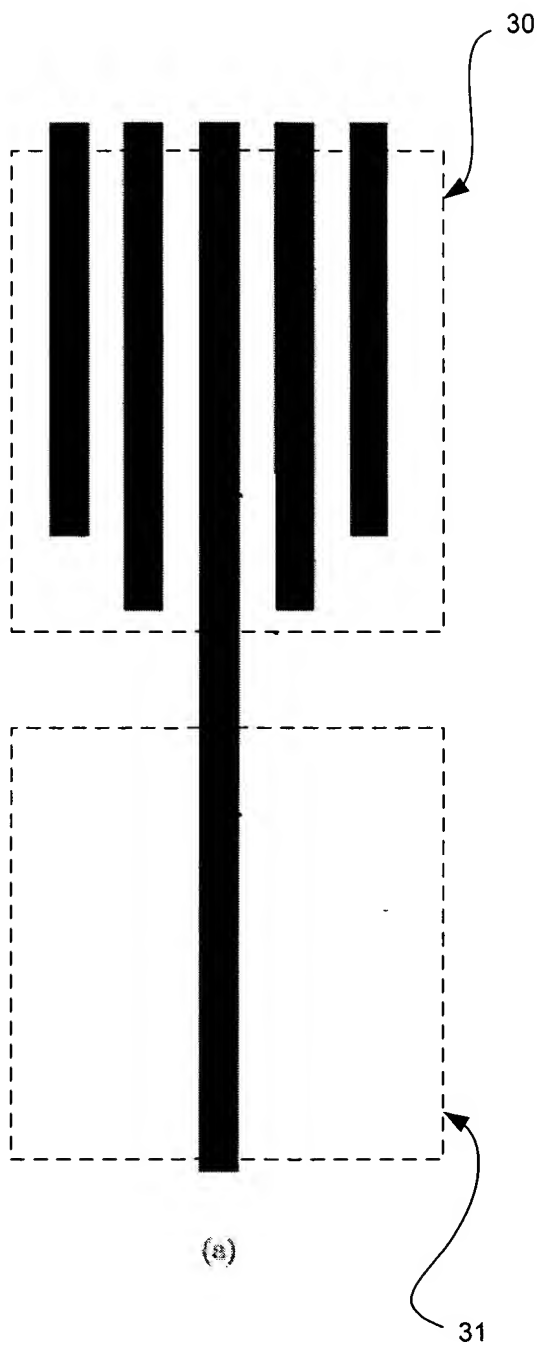


Figure 2a

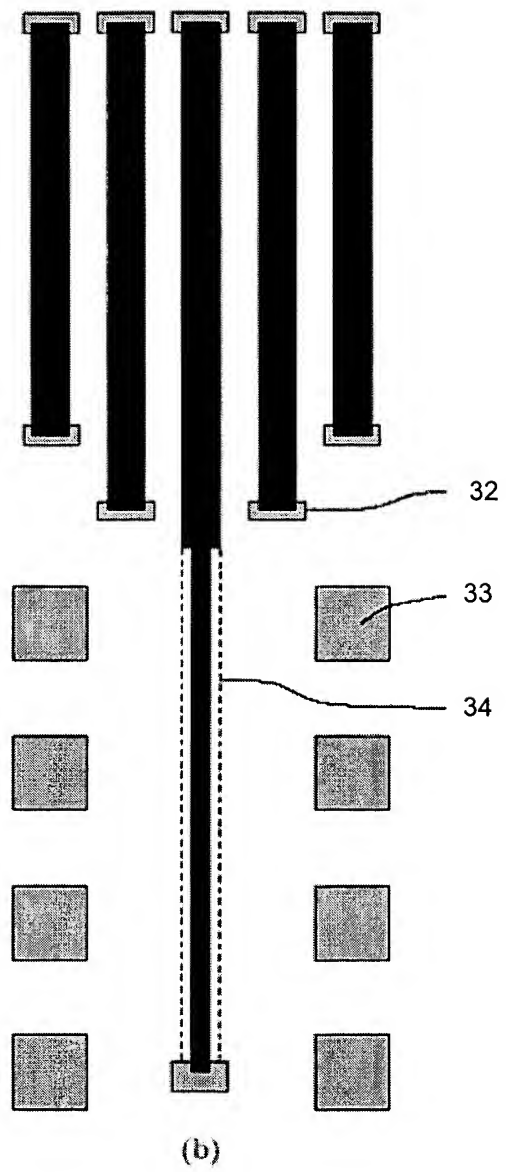


Figure 2b

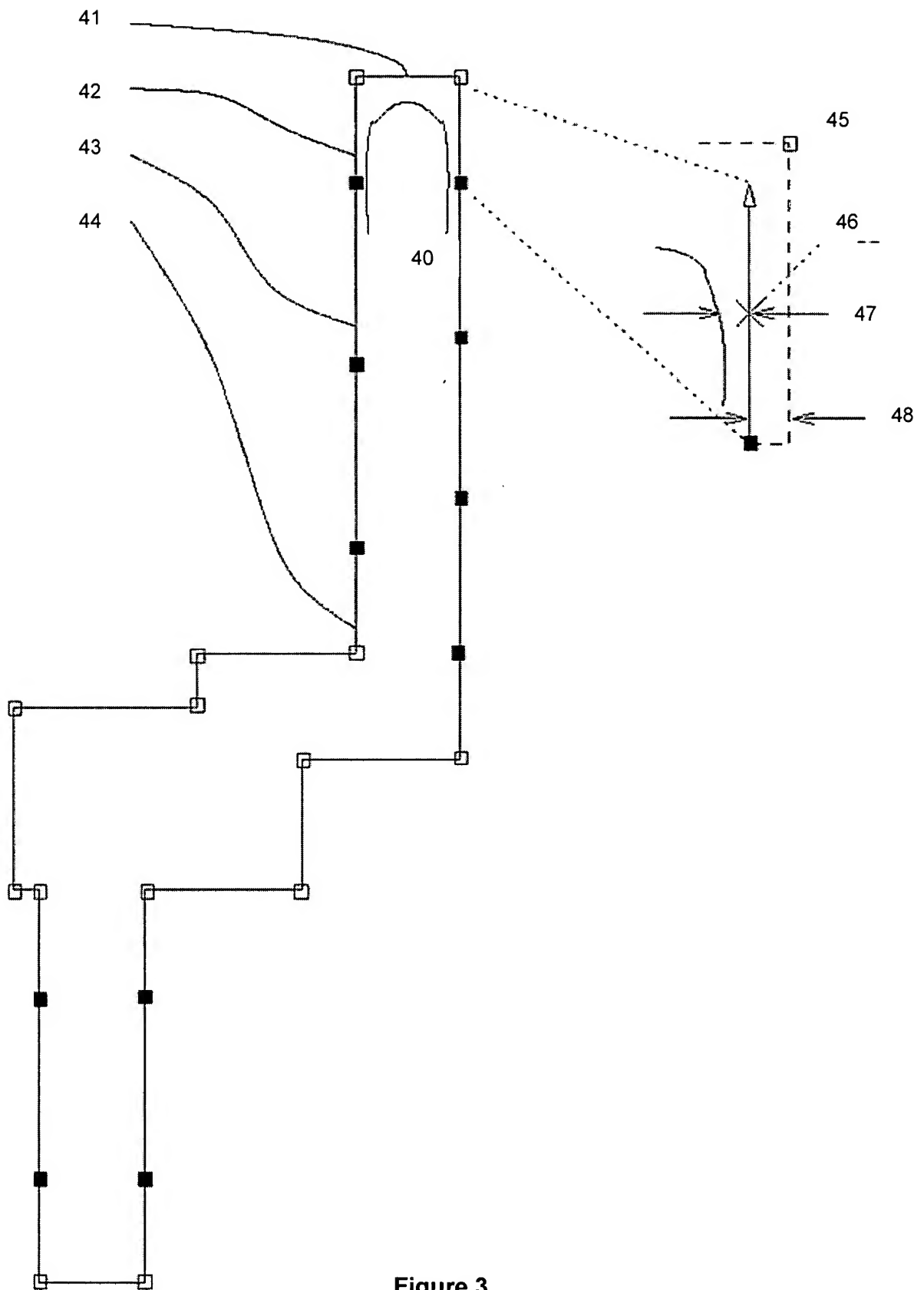


Figure 3

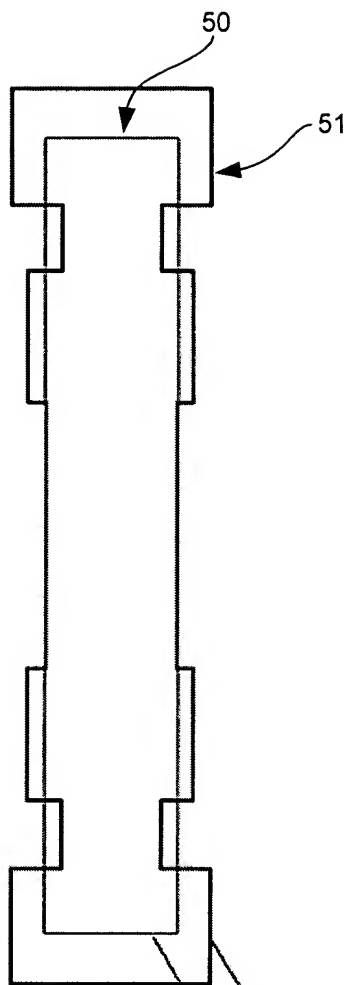


Figure 4a

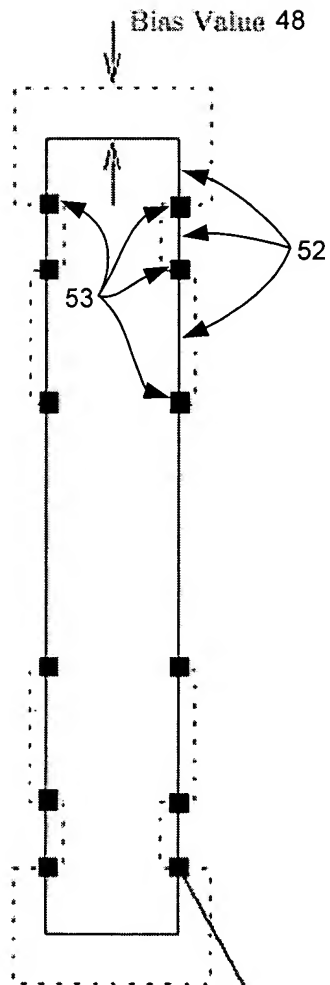


Figure 4b

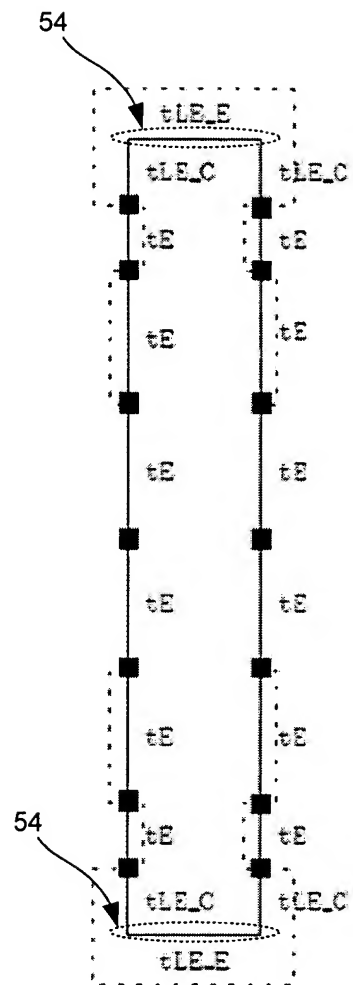


Figure 4c

OPC'ed Layer

Original Layer

Fragment Vertex 53

Constructing intermediate enhancement state layout

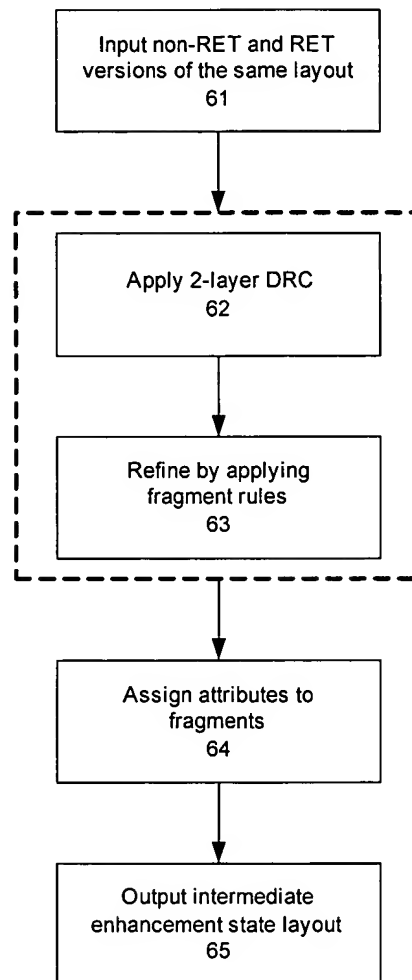


Figure 5a

Incremental OPC flow

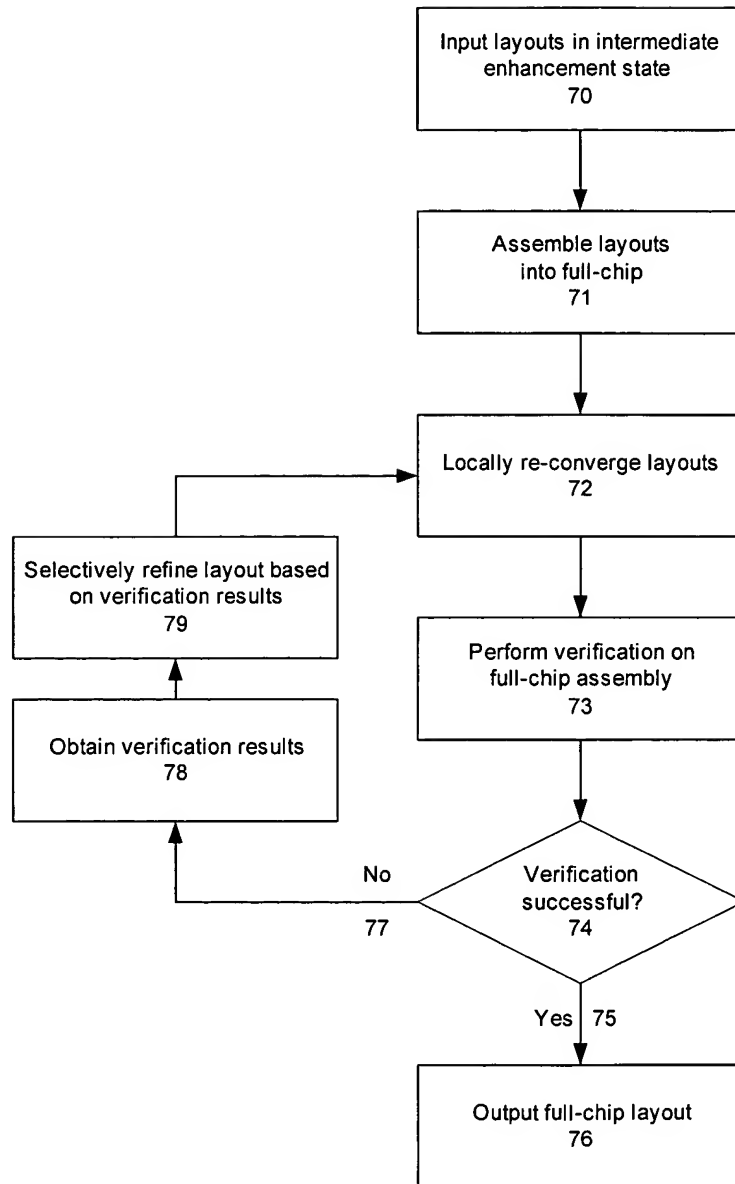


Figure 5b

Locally re-converging layouts

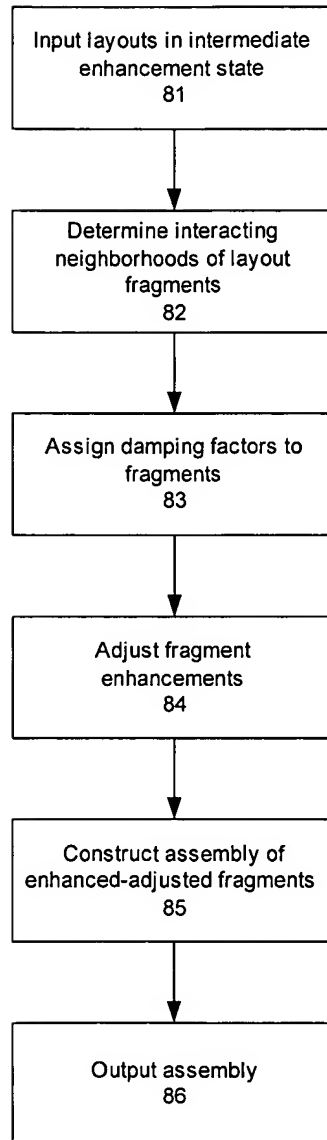


Figure 5c

Circuit Block 60	Circuit Block 60	Circuit Block 60
Circuit Block 60	Circuit Block 60	Circuit Block 60
Circuit Block 60	Circuit Block 60	Circuit Block 60

Figure 6